# Tutorials

There are a total of 12 tutorials this year on 12 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

***Ali Sheikholeslami***
*ISSCC Education Chair*

The presentations and the videos of all 12 tutorials (90 minutes each)
will be available online, on-demand, as of:
**Friday, Feb. 5, 2021, 5:00pm, PST**
**until March 31, 2021.**

**Live Q&A sessions for the tutorials will be available on:**
**Feb. 13, 2021, 7:00am - 9:00am PST**

20 minute live session = 5 minute summary + 10 minute Q&A + 5 minute break

The Q&A sessions will be recorded and made available after their live sessions.

## Live Q&A - February 13, 7:00am PST

## T1: Fundamentals of RF and mm-Wave Power-Amplifier Designs

**Hua Wang,** *Georgia Institute of Technology, Atlanta, GA*

This tutorial presents an overview of RF and mm-wave power-amplifier (PA) designs in silicon, focusing on the design fundamentals. First, the tutorial introduces PA performance metrics and their impact on wireless systems. Next, it presents the design basics of both PA active circuits and passive networks. The tutorial discusses popular PA classes, such as Class A, AB, B/C, E, F/F-1, and J. Finally, the tutorial concludes with several RF and mm-wave PA design examples.

**Hua Wang** is an associate professor at the School of Electrical and Computer Engineering at the Georgia Insitute of Technology and the director of the Georgia Tech Electronics and Micro-System (GEMS) lab. Prior to that, he worked at Intel Corporation and Skyworks Solutions. He received his M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, in 2007 and 2009, respectively.

Dr. Wang is interested in innovative analog, mixed-signal, RF, and mm-wave integrated circuits and hybrid systems for wireless communication, sensing, and bioelectronics applications. He has authored or co-authored over 170 peer-reviewed journal and conference papers.

Dr. Wang received the DARPA Director's Fellowship Award in 2020, the DARPA Young Faculty Award in 2018, the NSF CAREER Award in 2015, the Qualcomm Faculty Award 2020, and the IEEE MTT-S Outstanding Young Engineer Award in 2017. His GEMS research group has won multiple academic awards and best paper awards, including the 2019 Marconi Society Paul Baran Young Scholar, the IEEE RFIC Best Student Paper Awards (2014, 2016, and 2018), the IEEE CICC Outstanding Student Paper Awards (2015, 2018, and 2019), the IEEE CICC Best Conference Paper Award (2017).

## Live Q&A - February 13, 7:20am PST

## T2: Fundamentals of Memory Subsystem Design for HPC and AI

**Kyu-Hyoun (KH) Kim,** *IBM T. J. Watson, Yorktown Heights, NY*

This tutorial will help the audience understand memory subsystem design choices for various applications and systems: including technology, hierarchy, architecture, interface and packaging. The talk will begin with an overview of basics of memory subsystems including memory interfaces (device and module interfaces), controllers, subsystem architectures and RAS & ECC. The tutorial will then move on to explore memory subsystem design optimizations for HPC and AI applications.

**Kyu-Hyoun (KH) Kim** received his Ph.D. degree in EE from KAIST in 1997. In 1998, he joined Samsung Electronics and led the I/O circuit design team for DDR1/DDR2/DDR3 SDRAM and graphic memories.

He joined IBM T. J. Watson in 2006, and led memory subsystem development for IBM's HPC systems: including BlueGene and Exascale systems. He is now in charge of exploratory AI hardware.

He represents IBM in JEDEC for memory standardization. He received the JEDEC Technical Recognition Award in 2011 and an Award of Excellence in 2019.

Dr. Kim has presented eight papers at the International Solid-State Circuits Conference (ISSCC) as a first author between 1996 and 2009. He received the ISSCC Takuo Sugano Outstanding Paper Award in 2007. He holds 168 U.S. patents.

## Live Q&A - February 13, 7:40am PST

## T3: Silicon Photonics – from Basics to ASICs

**Sudip Shekhar,** *University of British Columbia, Vancouver, Canada*

The impact of silicon photonics is expected to grow exponentially in the next decade, driven by the demand for routing, switching, sensing, and computing massive amounts of data.

In this tutorial, the basics of silicon photonic devices will be first presented briefly. Then state-of-the-art examples of silicon photonics and CMOS circuits will be described for high-speed intensity-modulation and coherent links, router-switches, biomedical sensing, and compute accelerators.

**Sudip Shekhar** received his B.Tech. degree from the Indian Institute of Technology, Kharagpur, and the Ph.D. degree from the University of Washington, Seattle, in 2003 and 2008, respectively.

From 2008 to 2013, he was with the Circuits Research Laboratory, Intel Corporation, Hillsboro, OR, USA, where he worked on high-speed I/O architectures. He is currently an Associate Professor of Electrical and Computer Engineering with the University of British Columbia. His research interests include circuits for high-speed electrical and optical I/O interfaces, frequency synthesizers, and wireless transceivers.

Dr. Shekhar was a recipient of the IEEE Transactions on Circuit and Systems Darlington Best Paper Award in 2010 and a co-recipient of the IEEE Radio-Frequency IC Symposium Best Student Paper Award in 2015.

## Live Q&A - February 13, 8:00am PST

### T4: Measuring and Evaluating the Security Level of Circuits

**Ingrid Verbauwhede,** *KU Leuven, Leuven, Belgium*

When we design for low power, we estimate the power consumption at design time and measure it after fabrication and before we submit it to ISSCC. The same must be done with the security evaluation of a circuit: it should be estimated at design time, and measured after fabrication. It is however difficult to measure security. Therefore, in this tutorial, we plan to show how to perform the security evaluation for different classes of circuits: true random number generators, physically unclonable functions and side-channel evaluation of cryptographic implementations.

When designing a true random number generator, statistical tests on the output data are not sufficient: important in this context are the NIST standards SP800-90B and the German BSI AIS20/31 standards to evaluate true randomness. In the context of physically unclonable functions, established standards do not exist yet: here it is important to evaluate how much is the total cost to generate a full-entropy key. When evaluating the resistance to side-channel and fault attacks, it is important to describe the set-up of the experiments. If not, the only conclusion one can make is that the circuit resists an evaluation with the given set-up.

**Dr. Ir. Ingrid Verbauwhede** is a Professor in the COSIC research group of the Electrical Engineering Department of the KU Leuven. She is also adjunct professor at the University of California, Los Angeles. She received her PhD degree from the KU Leuven and was a post-doctoral researcher at UC Berkeley. At COSIC, she leads the secure embedded systems and hardware group. She is a Member of IACR and a Fellow of the IEEE. She was elected as member of the Royal Flemish Academy of Belgium for Science and the Arts in 2011. She is a recipient of an ERC Advanced Grant in 2016 and received the IEEE 2017 Computer Society Technical Achievement Award.

She is a pioneer in the field of efficient and secure implementations of cryptographic algorithms on many different platforms: ASIC, FPGA, embedded, cloud. With her research she bridges the gaps between electronics, the mathematics of cryptography and the security of trusted computing, including physically unclonable functions and true random number generators. Her group owns and operates an advanced electronic security evaluation lab. She is the author and co-author of more than 300 publications in conferences, journals, book chapters and books.

## Live Q&A - February 13, 8:20am PST

### T5: Calibration Techniques in ADCs

**Ahmed Ali,** *Analog Devices, Greensboro, NC*

Digitally assisted ADCs have become mainstream. Fine geometry processes and the insatiable need for higher resolution ADCs at higher sample rates have made sophisticated digital assistance a necessity. In this tutorial, we cover some of the advanced calibration techniques for high-speed and high-resolution ADCs. These include techniques to correct for inter-stage gain and settling errors, amplifier non-linearity, memory, DAC and reference errors. The tutorial will discuss the advantages and limitations of the different approaches, some of the practical considerations, and some state-of-the-art examples.

**Ahmed M. A. Ali** received the Ph.D. degree in electrical engineering from the University of Pennsylvania. He is a Fellow at Analog Devices, where he has led the design and development of several industry and world firsts in the high-speed data converter field. Before Analog Devices, he was with Texas Instruments and an Adjunct Assistant Professor at the University of Pennsylvania. He is an Associate Editor of the IEEE Transactions on Circuits and Systems I and was an SSCS Distinguished Lecturer. He is the author of the book: “High Speed Data Converters”, by the Institution of Engineering & Technology (IET).

## Live Q&A - February 13, 8:40am PST

## T6: Basics of DAC-Based Wireline Transmitters

**Friedel Gerfers,** *Technische Universität Berlin, Berlin, Germany*

This tutorial presents a practical overview of current-mode and voltage-mode DAC drivers, focusing on the fundamentals, accuracy challenges and design solutions.

First, the tutorial explains transmitter specifications for swing, jitter, equalization and linearity, while also introducing DAC performance metrics and discussing their overall impact on wireline systems.

Next, the current-mode and voltage-mode DAC architectures are introduced while highlighting the pros and cons of each. High-speed design challenges, bandwidth and non-linearity trade-offs are reviewed. PVT and mismatch effects, swing enhancements and calibration techniques are introduced.

The tutorial concludes with several DAC design examples utilizing deep submicron CMOS technologies reaching up to 56Gbaud/s.

**Friedel Gerfers** is a full professor in the Computer Engineering and Microelectronics Department at the Technische Universität Berlin, Germany and holds the Einstein-Professorship for Mixed-Signal Circuit Design.

He received the Dr.-Ing. degree from the Albert-Ludwigs-University Freiburg, Germany, in 2005.

Thanks to his entrepreneurial spirit, he co-founded two the technology start-ups in 2009 and 2018: NiederRhein Technologies, in Mountain View, USA and IC4X GmbH, in Berlin, Germany, which specialize in the development of high-performance analog and mixed-signal circuits and systems.

Prof. Gerfers is an author of the book “Continuous-Time Sigma-Delta A/D conversion, Fundamentals, Error Correction and Robust Implementations”.

## Live Q&A - February 13, 7:00am PST

## T7: Basic Design Approaches to Accelerating Deep Neural Networks

**Rangharajan Venkatesan,** *NVIDIA, Sunnyvale, CA*

Deep neural networks are used across a wide range of applications. Custom hardware optimizations for this field offer significant performance and power advantages compared to general-purpose processors. However, achieving high TOPS/W and/or TOPS/mm$^2$ along with the requirements for scalability and programmability is a challenging task.

This tutorial presents various design approaches to strike the right balance between efficiency, scalability, and flexibility across different neural networks and towards new models. It presents a survey of (i) different circuits and architecture techniques to design efficient compute units, memory hierarchies, and interconnect topologies, (ii) compiler approaches to effectively tile computations, and (iii) neural network optimizations for efficient execution on the target hardware.

**Rangharajan Venkatesan** is a Senior Research Scientist at NVIDIA. He received his B.Tech. degree in Electronics and Communication Engineering from the Indian Institute of Technology, Roorkee in 2009 and his Ph.D. degree in Electrical and Computer Engineering from Purdue University in 2014. His research interests include machine learning accelerators, high-level synthesis, spintronic memories, and SoC design methodologies. Dr. Venkatesan’s paper on scalable deep-learning accelerator design received the Best Paper Award at the International Symposium on Microarchitecture (MICRO), 2019. His work on spintronic memory design was recognized with the Best Paper Award at the International Symposium on Low Power Electronics and Design (ISLPED), 2012 and a Best Paper nomination at the Design, Automation and Test Conference and Exhibition (DATE) in Europe, 2017. Dr. Venkatesan’s work on FinFET-based SRAM also received a Best paper nomination at the Design, Automation and Test Conference and Exhibition (DATE) in Europe, 2015. Dr. Venkatesan has been a member of the technical program committees of several leading IEEE conferences including the International Solid-State Circuits Conference (ISSCC), the International Symposium on Microarchitecture (MICRO), the Design Automation Conference (DAC), and the International Symposium on Low Power Electronics and Design (ISLPED).

## Live Q&A - February 13, 7:20am PST

## T8: On-Chip Interconnects: Basic Concepts, Designs, & Future Opportunities

**Yvain Thonnart,** *CEA-List, Grenoble, France*

On-chip communication impacts the performance, energy efficiency, and area of systems-on-chip, multi-processors and highly parallel accelerators. This tutorial introduces a range of design options for on-chip interconnects. It presents routing schemes and mapping of different protocol families, flow-control and arbitration, synchronization strategies across clock domains, and fully asynchronous circuits. Finally, it introduces the potential of 3D-chip integration for on-chip communication.

**Yvain Thonnart** graduated from the Ecole Polytechnique and received the MS degree in 2005 from Telecom ParisTech, France. In 2005, He joined the Technological Research Division of CEA, the French Alternative Energies and Atomic Energy Commission, within CEA-Leti until 2019, then within CEA-List. He is now senior expert on communication & synchronization in systems-on-chip, and scientific advisor for the mixed-signal lab. His main research interests include asynchronous logic, networks-on-chip, physical implementation, emerging technologies integration, and interposers. He has contributed to and led several digital circuits projects, and co-authored more than 60 technical papers and 10 patents.

## Live Q&A - February 13, 7:40am PST

## T9: Designing Amplifiers for Stability

**Viola Schaffer,** *Texas Instruments, Freising, Germany*

Most amplifier designers spend at least as much or more effort assuring stability under all operating conditions with proper frequency compensation than on other amplifier features. This tutorial will revisit the basics of frequency compensation such as Miller, parallel, nested-Miller and feed-forward compensation and compare them in terms of power efficiency and load-drive capabilities. We will look into the loading effects of subsequent stages, common design traps and round up with a case study of recently published amplifiers.

**Viola Schäffer** was born in Szeged, Hungary in 1974. She received the M.S. degree in electrical engineering from the University of Arizona, Tucson in 1999.

She joined Texas Instruments Incorporated (formerly Burr-Brown Corporation) in 1998 and has been working as an analog IC design engineer/manager at various locations including Tucson, Arizona, as well as Erlangen and Freising in Germany. She was elected Distinguished Member Technical Staff in 2018. Her work focuses on precision signal conditioning including instrumentation and programmable-gain amplifiers, power amplifiers, industrial drivers as well as magnetic-based current sensors. She holds 17 patents related to this work with several applications pending.

## Live Q&A - February 13, 8:00am PST

## T10: Fundamentals of Fully Integrated Voltage Regulators

**Yan Lu,** *University of Macau, Macao, China*

Fully integrated voltage regulators (FIVRs) enable fast dynamic voltage and frequency scaling for energy-efficient high-performance digital systems. This tutorial will cover the fundamentals of low-dropout regulators (LDOs), as well as switched-capacitor (SC) and inductor-based DC-DC converters. Emphasis will be put on design considerations of analog/digital/mixed control, PID control for FIVR, resonant SC, and hybrid DC-DC converters. Last but not least, we will have a brief review of distributed FIVR designs.

**Yan Lu** received his B.E. and M.Sc. degrees in Microelectronics from South China University of Technology, and his Ph.D. degree in Electronic and Computer Engineering from the Hong Kong University of Science and Technology (HKUST). Since 2014, he has been with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, where he is now an Associate Professor.

His research interests include fully integrated voltage regulators, DC-DC converters, and wireless power transfer. He is a recipient/co-recipient of the IEEE SSCS Pre-Doctoral Achievement Award, the IEEE CAS Society Outstanding Young Author Award, and the ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper. He is currently a member of the Technical Program Committee of ISSCC and CICC.

### Live Q&A - February 13, 8:20am PST

## T11: Ultra-Low-Power Wireless-Receiver Design

**David D. Wentzloff,** *University of Michigan, Ann Arbor, MI*

Pervasive-computing and new wireless-sensing applications have re-energized the need for ultra-low-power (ULP) radios and wakeup receivers (WuR). These are used to improve the efficiency of wireless networks in multiple ways. This talk covers recent trends in ULP wireless receiver design, ULP receiver implementations, and design tradeoffs with examples of common ULP receiver architectures as well as examples of how industry wireless standards are adopting signaling to support ULP receivers.

**David Wentzloff** received a BS in Electrical Engineering from the University of Michigan, and a Ph.D. in Electrical Engineering from MIT. Since 2007, he has been with the University of Michigan, where he is currently an Associate Professor of Electrical Engineering and Computer Science. His research focuses on RF integrated circuits, with an emphasis on ultra-low-power design. In 2012, he co-founded Everactive; a fabless semiconductor company developing ultra-low-power wireless SoCs, where he is currently a co-CTO.

### Live Q&A - February 13, 8:40am PST

## T12: Brain Computer Interfaces: Fundamentals to Future Technologies

**Rikky Muller,** *University of California, Berkeley, CA*

Fueled by recent major investments, brain computer interfaces (BCIs) stand to revolutionize the treatment of neurological conditions, and in the future, the human experience. This tutorial will highlight key challenges in the realization of implantable BCIs such as closed-loop operation, miniaturization, and scale. We will start by covering fundamental circuit building blocks and their interactions with electrodes, signals, and tissues. We will then go through an example of how to minimize the volume of a wireless implant.

**Rikky Muller** is an Assistant Professor of Electrical Engineering and Computer Sciences at UC Berkeley where she holds the S. Shankar Sastry Professorship in Emerging Technologies. She is a Co-director of the Berkeley Wireless Research Center (BWRC), a Core Member of the Center for Neural Engineering and Prostheses and an Investigator at the Chan-Zuckerberg Biohub. Her research group focuses on emerging implantable and wearable medical devices and in developing low-power, wireless microelectronic and integrated systems for neurological applications. Prof. Muller was also the Co-founder of Cortera Neurotechnologies, a medical device company focused on closed-loop deep brain stimulation technology that was founded in 2013 and acquired in 2019.